#14/Cl
8-1-00
Mharrison

Response Under 37 CFR 1.116
Expedited Procedure
Examining Group: 2811

ENTER
2-24-01
Robertson

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

AMENDMENT "C"

APPLICANT:	Ohsawa et al	
SERIAL NO.:	09/199,305	GROUP ART UNIT: 2811
DATE FILED:	November 25, 1998	EXAMINER: L. Thai
INVENTION:	"A SEMICONDUCTOR DEVICE AND AN ELECTRICAL DEVICE USING THE SEMICONDUCTOR DEVICE"	

Assistant Commissioner for Patents
Washington, D.C. 20231

S I R:

In response to the **FINAL REJECTION** dated April 25, 2000, please amend the above-identified application as follows:

IN THE CLAIMS:

Please cancel non-elected claims 6-10, without prejudice.

please enter

Please amend claim 15 to read as follows:

--15. (Amended) A semiconductor device [according to claim 1, wherein] comprising:

a plurality of wiring films formed on a front surface of a base comprising an insulating resin and having electrode-forming holes, the surfaces of the wiring films and the surface of the base being positioned on the same plane and at least parts of the wiring films overlapping with the electrode-forming holes;

a conductive material embedded into the electrode-forming holes to form external electrodes on the back surface, away from the wiring films, of the base;

please enter LT.

a semiconductor element positioned on said front surface of the base with an insulating film therebetween, the back surface of the semiconductor element being bonded to said front surface of the base; and

wires for bonding the electrodes of the semiconductor element to the corresponding wiring films, the wiring films [are] being formed by a layer of copper covered by a nickel layer so that the wires are bonded to the nickel layer.--

Cancel C1

REMARKS

Claims 1-5 and 11-15 are presented for reconsideration.

In the **Final Rejection**, it is noted that the proposed drawing corrections filed on February 22, 2000 were approved; claims 1-3 were rejected under 35 USC 102(e) as being anticipated by Chia et al; claims 1-3 were also rejected under 35 USC 102(e) as being anticipated by Distefano et al; claims 11 and 12 were rejected under 35 USC 103 as being unpatentable over Chia et al or Distefano et al; claims 4 and 13 were rejected under 35 USC 103(a) as being unpatentable over Chia et al and/or Distefano et al in view of McCormick et al; claim 5 was rejected under 35 USC 103 as being unpatentable over Chia et al in view of Shim et al; claims 14 and 15 were rejected under 35 USC 103 as being unpatentable over Chia et al or Distefano et al in further view of the newly-cited patent to Tagusa et al.

By this amendment, the non-elected method claims 6-10 have been cancelled, with applicants reserving the right to file a divisional application and claim 15, which was dependent on claim 1, has been amended to be an independent claim including all of the limitations of claim 1.

It is respectfully requested that this amendment be entered for purposes of placing the application in condition for immediate formal allowance or in better form for an Appeal. It is noted that no changes in the claims have been made and, thus, no new issues have been raised.

In the Final Rejection, the Examiner has repeated the rejections under 35 USC 102 based on Chia et al or Distefano et al. It is respectfully submitted that neither of these references teaches or suggests the structure recited in claims 1-3, either by anticipating it under 35 USC 102(e) or rendering it obvious under 35 USC 103. As pointed out in the previous amendment, Chia et al does not teach or suggest the claimed structure. Chia et al, in Fig. 2, shows a substrate 10, which, on a front surface, has contact films 12 and has a chip 20 mounted thereon. The substrate 10 has conductive vias 16 which extend to contacts 14 on the bottom or back surface of the substrate. These contacts 14 are in contact with solder balls 18 and the entire surface thereof is then covered with a solder mask layer 22. It is submitted that, contrary to the Examiner's discussion of this reference and his additional element numbers, the reference does not teach wiring films on a front surface of the base 10, the surface of the wiring films and the surface of the base being positioned on the same plane. It is also submitted that the Examiner's interpretation that the solder mask 22 is the base would then not have the semiconductor element positioned on said front surface of the base. For these reasons, it is submitted that claim 1 is clearly not anticipated by Chia et al. It is also submitted that to interpret the teachings of this reference as proposed by the Examiner is strictly using hindsight that is not taught by the reference and is completely misrepresenting the teachings of the reference. Therefore, it is submitted that claims 1-3 are clearly patentable and allowable over Chia et al.

With regard to the rejection of claims 1-3 on Distefano et al, it is submitted that the substrate in Fig. 3F, which supports the chip 10 and conductors 50 on the front surface, does not teach or suggest the films formed on the front surface of a base, surfaces of the wiring films and the surface of the base being positioned in the same plane, as recited in claim 1. Therefore, claims 1, 2 and 3 are clearly not anticipated by this reference and are allowable. With regard to the embodiment illustrated in Fig. 3G of Distefano et al, the insertion of element number 50' and 30' seem contrary to the disclosure of the reference and, thus, there is no teaching or suggestion of the wirings, such as 50 being on the front surface of the base 30, which front surface also supports the chip 10. In other words, the interpretation of the embodiment of Fig. 3G completely disregards the teachings of the reference and has an interpretation based solely on applicants'

disclosure. Thus, it is submitted that claims 1-3 are clearly not anticipated by this reference and are allowable.

With regard to the rejection of claims 11 and 12 on either Chia et al or Distefano et al, it is submitted that the deficiencies mentioned hereinabove with regard to the rejection of claims 1-3 is still present and, therefore, claims 11 and 12 are clearly patentable over the teachings of these two references and are allowable.

With regard to the rejection of claims 4 and 13, it is submitted that while McCormick et al may teach adding the reinforcement elements, such as 210 of Fig. 2B, it does not teach or suggest the basic deficiencies with the primary references. Therefore, even if it were combinable with the two primary references, it would not teach the structure recited in claims 4 and 13.

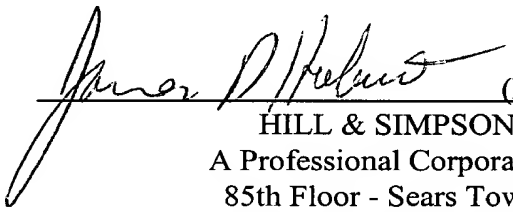
With regard to the rejection of claim 5 on Chia et al in view of Shim et al, it is again pointed out that Shim et al does not teach or suggest the vents as alleged in the Office Action. The holes 23 are described in the reference as plated through-holes, and there is no suggestion of these holes being vents without relying on applicants' disclosure to suggest such a modification. In other words, it is submitted that a person of ordinary skill in the art having plated through-holes would not consider those as vents without relying on applicants' disclosure. Thus, it is submitted that claim 5 is clearly patentable over the teachings of the reference.

With regard to the rejection of claims 14 and 15, it is noted that the newly-cited reference to Tagusa et al is concerned with connecting electronic components, such as 25, to a substrate, such as 28, of a transparent glass or other material and wiring layers 27 which have previously been described as being transparent conductive films, such as indium tin oxide, and that these layers are then covered with a nickel or other metal to improve the wetability of the solder 31. It is also noted that, as pointed out on lines 56-60 of column 2, this is proved to be entirely unsatisfactory. Therefore, it is submitted that a person of ordinary skill in the art having

both Chia et al and Tagusa et al would not find that the wiring films are formed of copper covered by a nickel layer, as recited in claims 14 and 15. It is submitted that the combination applied against these two claims is an improper combination, since there is no teaching or suggestion in the two references to make the substitution and combination as proposed by the Examiner. The only teaching of this is applicants' disclosure and, therefore, the combination is based solely on hindsight, which is contrary to the Patent Laws. It is also submitted that even if the combination were proper, there is no teaching or suggestion in the two references of forming the film as a copper layer covered by a nickel layer, since the secondary reference to Tagusa et al only talks about applying a nickel layer on an indium tin oxide film. Therefore, it is respectfully submitted that claims 14 and 15 are clearly patentable over the prior art and are allowable.

In view of the amendments and explanations contained hereinabove, it is respectfully submitted that this application is now in condition for immediate formal allowance and further reconsideration to that end is earnestly solicited.

Respectfully submitted,



(Reg. No. 24,149)

HILL & SIMPSON
A Professional Corporation
85th Floor - Sears Tower
Chicago, Illinois 60606

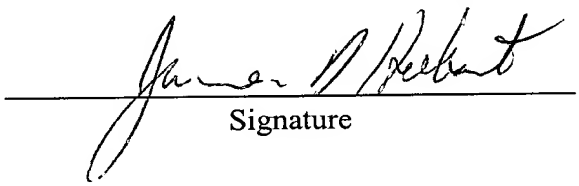
Telephone: (312) 876-0200 - Ext. 647

DATED: July 25, 2000

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231 on July 25, 2000.

James D. Hobart
Name of Applicant's Attorney



Signature

July 25, 2000
Date